5547 90200

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 3/27/03 Serial # 10/015,757 Priority Application Date 12/22/00

Your Name M. Lewis Examiner # _____

AU 2822 Phone 305-3743 Room Plaza 3-3B07

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

03-28-03 P12:54 IN

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Bode, I would like to get an updated search.
Claims 1-11

Problem: See Page 1 lines 14-27
" 2 " 1-26

Solution: " " " " 1-19

Staff Use Only

Searcher: Bode

Searcher Phone: 605-1706

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 03-31-03

Date Completed: 03-31-03

Searcher Prep/Rev Time: 60

Online Time: 240

Type of Search

Structure (#) _____

Bibliographic ✓

Litigation _____

Fulltext ✓

Patent Family _____

Other _____

Vendors

STN ✓

Dialog ✓

Questel/Orbit _____

Lexis-Nexis _____

WWW/Internet _____

Other _____

```
Set     Items   Description
S1     227003   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
            GRATED()CIRCUIT?
S2     996358   PREVENT? OR AVOID? OR PRECLUD? OR PROHIBIT? OR REDUC? OR E-
            LIMINAT?
S3     215367   CORROSION? OR DECAY? OR RUST? OR DETERIORAT? OR DECOMPOS? -
            OR OXIDI?ATION
S4      43647   CMP OR CHEMICAL()MECHANICAL()(POLISH? OR PLANAR?) OR POLIS-
            H? OR PLANARI?
S5       7878   (WIRE OR MAIN OR DUMMY OR FINE  OR PAD OR PADS)(3N)PATTERN?
S6          3   S1(S)S2(S)S3(S)S4(S)S5
S7         32   S1(S)S2(S)S3(S)S5
S8         14   S7 AND IC=H01L?
S9         12   S8 NOT S6
S10        10   S1(10N)S3(10N)S5
S11         7   S10 NOT (S6 OR S9)
? show files
File 348:EUROPEAN PATENTS 1978-2002/Sep W05
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20021003,UT=20020926
         (c) 2002 WIPO/Univentio
?
```

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Set     Items   Description
S1    1157184   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
            GRATED()CIRCUIT?
S2    7250879   PREVENT? OR AVOID? OR PRECLUD? OR PROHIBIT? OR REDUC? OR E-
            LIMINAT?
S3     502770   CORROSION? OR DECAY? OR RUST? OR DETERIORAT? OR DECOMPOS? -
            OR OXIDI?ATION
S4     616740   CMP OR CHEMICAL()MECHANICAL()(POLISH? OR PLANAR?) OR POLIS-
            H? OR PLANARI?
S5       3788   (WIRE OR MAIN OR DUMMY OR FINE  OR PAD OR PADS)(3N)PATTERN?
S6          1   S1(S)S2(S)S3(S)S4(S)S5
S7          2   S1(S)S2(S)S3(S)S5
S8          2   S6 OR S7
S9          2   RD (unique items)
S10      9318   S2(N)S3
S11         4   S1(S)S10(S)S4
S12         4   S11 NOT S9
? show files
File 647:CMP  Computer Fulltext 1988-2002/Sep W4
         (c) 2002 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2002/Oct 09
         (c) 2002 The Dialog Corp.
File  98:General Sci Abs/Full-Text 1984-2002/Sep
         (c) 2002 The HW Wilson Co.
File 624:McGraw-Hill Publications 1985-2002/Oct 09
         (c) 2002 McGraw-Hill Co. Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2002/Oct 09
         (c) 2002 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2002/Oct 10
         (c) 2002 The Gale Group
File 484:Periodical Abs Plustext 1986-2002/Oct W1
         (c) 2002 ProQuest
File  95:TEME-Technology & Management 1989-2002/Oct W1
         (c) 2002 FIZ TECHNIK
File  16:Gale Group PROMT(R) 1990-2002/Oct 10
         (c) 2002 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File 148:Gale Group Trade & Industry DB 1976-2002/Oct 10
         (c)2002 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2002/May
         (c) 2002 The HW Wilson Co
File 583:Gale Group Globalbase(TM) 1986-2002/Oct 10
         (c) 2002 The Gale Group
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2002/Oct 10
         (c) 2002 Business Wire.
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2002/Oct 10
         (c) 2002 PR Newswire Association Inc
?
```

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Set     Items   Description
S1    1190763   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
            GRATED()CIRCUIT?
S2    5159509   PREVENT? OR AVOID? OR PRECLUD? OR PROHIBIT? OR REDUC? OR E-
            LIMINAT?
S3     544973   CORROSION? OR DECAY? OR RUST? OR DETERIORAT? OR DECOMPOS? -
            OR OXIDI?ATION
S4      98179   CMP OR CHEMICAL()MECHANICAL()(POLISH? OR PLANAR?) OR POLIS-
            H? OR PLANARI?
S5      23590   (WIRE OR MAIN OR DUMMY OR FINE  OR PAD OR PADS)(3N)PATTERN?
S6          8   S1 AND S2 AND S3 AND S4 AND S5
S7      21720   S1 AND S2 AND S3
S8        172   S7 AND S5
S9         66   S7(4N)S5
S10        41   S7(2N)S5
S11        33   S10 AND PY<=2000
S12        62   S9 AND IC=H01L?
S13         6   S8 AND IC=H01L-027/10
S14         6   S13 NOT S11
S15    105019   S2(2N)S3
S16     52771   S2(N)S3
S17        39   S16 AND S1 AND S5
S18        31   S17 NOT (S11 OR S14)
S19        27   S18 AND IC=H01L?
?show files
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200264
         (c) 2002  Thomson Derwent
?
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... a conductive resist 6 is formed on the main surface and rear surface of a **semiconductor** substrate by spin-coating a conductive resist 6. Then, a photoresist 4 is subjected to **patterning** onto the **main** surface of this **semiconductor** substrate. Then, by implanting impurities such as As(sup +) by ion implantation, n(sup +) diffusion...

19/3,K/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03154436 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 02-129936 [JP 2129936 A]
PUBLISHED: May 18, 1990 (19900518)
INVENTOR(s): SUGIZAKI YOSHIAKI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-283354 [JP 88283354]
FILED: November 09, 1988 (19881109)
JOURNAL: Section: E, Section No. 961, Vol. 14, No. 365, Pg. 15, August 08, 1990 (19900808)

SEMICONDUCTOR DEVICE

INTL CLASS: **H01L-021/60**

ABSTRACT

PURPOSE: To **avoid** **corrosion** of a wiring and degradation of a bonding strength by a method wherein a bonding...
... a bonding ball over its whole surface and the bonding ball is bonded to a **dummy** **pattern** .

...

...The shape of a bonding pad 3 which is formed on the surface of a **semiconductor** chip 1 and is not covered with a protective film 4 is so formed as...

... bonding wire 5 bonded to the upper surface of the bonding pad 3. Further, a **dummy** **pattern** 7 which can be jointed with the bonding ball 6 is provided around the bonding...

...6 cover the whole surface of the bonding pad 3 and a part of the **dummy** **pattern** 7. With this constitution, the corrosion of a wiring 2 and the degradation of a

19/3,K/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

02349970 **Image available**
TRANSMITTING TYPE OPTICAL SENSOR

PUB. NO.: 62-266870 [JP 62266870 A]
PUBLISHED: November 19, 1987 (19871119)
INVENTOR(s): NAKAYAMA SHOICHIRO
NOGUCHI SHIGERU
WATANABE KANEO
KURIYAMA HIROYUKI
NAKAJIMA SABURO
NAKANO SHOICHI
KUWANO YUKINORI
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-111052 [JP 86111052]
FILED: May 15, 1986 (19860515)

JOURNAL: Section: E, Section No. 606, Vol. 12, No. 150, Pg. 162, May 10, 1988 (19880510)

INTL CLASS: **H01L-027/14** ; **H01L-031/10** ; H04N-005/335

ABSTRACT

PURPOSE: To **prevent** **deterioration** in electric characteristics and reliability due to corrosion at the contact part between a light...

... conductive oxide (TCO) and a rear electrode and to obtain the rear electrode of a **fine** **pattern** , by constituting the extended part of the rear electrode, which is coupled with the interconnection...

...selected among Pt, Pd, Cu, Al, Cr, and Ag, from the part contacting with a **semiconductor** film 4. The electrode 5 is constituted by a laminated body, in which the following layers are laminated: i.e. a first metal layer 5(sub 1) protecting the **semiconductor** film 4; a stable second metal layer 5(sub 2) including at least titanium (Ti...

19/3,K/11 **(Item 11 from file: 347)**

DIALOG(R)File 347:JAPIO

02115736 **Image available**

SEMICONDUCTOR DEVICE

PUB. NO.: 62-032636 [JP 62032636 A]

PUBLISHED: February 12, 1987 (19870212)

INVENTOR(s): KONDO HIDEYUKI

APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 60-172661 [JP 85172661]

FILED: August 05, 1985 (19850805)

JOURNAL: Section: E, Section No. 522, Vol. 11, No. 212, Pg. 17, July 09, 1987 (19870709)

SEMICONDUCTOR DEVICE

INTL CLASS: **H01L-023/48** ; **H01L-021/60**

ABSTRACT

PURPOSE: To **prevent** **corrosion** of a second bonding pad layer at the place of a through hole beneath a thin metal wire and to **prevent** **corrosion** of a first bonding pad layer, which is continued from the second layer, by connecting...

... in the interlayer insulating film 7. An aluminum film is deposited. The aluminum film is **patterned** and second bonding **pad** layer 9 is formed. At this time, the first and second bonding pad layers 4...

19/3,K/12 **(Item 12 from file: 347)**

DIALOG(R)File 347:JAPIO

01815956 **Image available**

MULTILAYER INTERCONNECTION STRUCTURE

PUB. NO.: 61-030056 [JP 61030056 A]

PUBLISHED: February 12, 1986 (19860212)

INVENTOR(s): TSUNODA NOBUHIKO
NAITO NOBORU
WADA TSUTOMU

APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 59-150789 [JP 84150789]

FILED: July 20, 1984 (19840720)

JOURNAL: Section: E, Section No. 415, Vol. 10, No. 184, Pg. 20, June 27, 1986 (19860627)

EP 1211716 A2 20020605 EP 2001127063 A 20011114 200246 B
US 20020068394 A1 20020606 US 2001986059 A 20011107 200246
JP 2002170953 A 20020614 JP 2000368661 A 20001204 200254

Priority Applications (No Type Date): JP 2000368661 A 20001204
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 1211716 A2 E 24 H01L-021/28
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 20020068394 A1 H01L-021/338
JP 2002170953 A 16 H01L-029/78
Semiconductor **device fabrication e.g. for MOS transistor, involves removing** dummy **gate** pattern **and silicon nitride film in contact plug formation region to form trenches that are filled...**

Abstract (Basic):
... A side wall insulating film of silicon oxide is formed in a **dummy** gate **pattern** on a **semiconductor** substrate (11) with an intervention of gate insulating film. An interlayer insulating film (22) is...
... An INDEPENDENT CLAIM is included for **semiconductor** device...

... **Semiconductor** device fabrication for **preventing deterioration** of gate insulating film in MOS transistor...

...Electrically conductive film is formed before the formation of the **dummy** gate **pattern** , the gate insulating film is not exposed but covered with electrically conductive film during the...

...The figure shows the schematic sectional view of the **semiconductor** device fabrication process in MOS transistor...

... **Semiconductor** substrate (11
Title Terms: **SEMICONDUCTOR** ;
International Patent Class (Main): **H01L-021/28** ...

... **H01L-021/338** ...

... **H01L-029/78**
International Patent Class (Additional): **H01L-021/3205** ...

... **H01L-021/336** ...
... **H01L-021/4763** ...

... **H01L-021/768**

19/3,K/17 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014425270 **Image available**
WPI Acc No: 2002-245973/200230
XRPX Acc No: N02-190753
Wire bonding method for semiconductor **package in which input-output pads of stacked** semiconductor **device are connected to mutually different conductive patterns using electroconductive wires**
Patent Assignee: AMKOR TECHNOLOGY KOREA INC (AMKO-N); HAN B J (HANB-I); KIN J D (KINJ-I); PARK Y K (PARK-I)
Inventor: HAN B J; KIM J D; PARK Y G; KIN J D; PARK Y K
Number of Countries: 003 Number of Patents: 003
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 2001189415 A 20010710 JP 2000309733 A 20001010 200230 B
KR 2001064907 A 20010711 KR 9959329 A 19991220 200230
US 20020064905 A1 20020530 US 2000745265 A 20001220 200240

Priority Applications (No Type Date): KR 9959329 A 19991220

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 2001189415 A   8 H01L-025/065
KR 2001064907 A   H01L-021/60
US 20020064905 A1   H01L-021/48
Wire bonding method for semiconductor **package in which input-output pads of stacked** semiconductor **device are connected to mutually different conductive patterns using electroconductive wires**

Abstract (Basic):
... 24) is formed around chip mounting area on a resin layer (22). A set of **semiconductor** chips (2,4) are stacked in the chip mounting area. A set of conductive patterns are formed near periphery of that area. The input-output pads (2a,4a) of the **semiconductor** chips are connected to the conductive **patterns** such that **pads** of each chip is connected to different patterns using electroconductive wires.
... An INDEPENDENT CLAIM is also included for **semiconductor** package...

...For stacked type **semiconductor** package or multi-chip module...

... **Prevents deterioration** of wire used for bonding, thereby improving durability of wire bond. Eliminates need for electroconductive...

...The figure shows the process for performing the bonding of a **semiconductor** chip with electroconductive wire...
... **Semiconductor** chips (2,4
...Title Terms: **SEMICONDUCTOR** ;
International Patent Class (Main): **H01L-021/48** ...

... **H01L-021/60** ...

... **H01L-025/065**
International Patent Class (Additional): **H01L-025/07** ...

... **H01L-025/18**

19/3,K/18 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014355101 **Image available**
WPI Acc No: 2002-175802/200223
XRPX Acc No: N02-133384
Inspection apparatus has illumination unit that irradiates light to antireflective coating of test object in quantity with which ultraviolet absorption of antireflective coating is saturated
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 2002014053 A 20020118 JP 2000195064 A 20000628 200223 B

Priority Applications (No Type Date): JP 2000195064 A 20000628
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 2002014053 A   10 G01N-021/956

Abstract (Basic):
... For inspecting condition of resist pattern formed on **semiconductor wafer** in lithography process in **semiconductor** processing...
... **Prevents deterioration** of measurement accuracy resulting from irradiation amount of illumination light. Enables accurate inspection of minute resist **pattern** since **wire** -width measurement of resist pattern is performed where the ultraviolet absorption of antireflective coating is
...International Patent Class (Additional): **H01L-021/027** ...

each other; (d) a **dummy pattern** formed on the insulating layer between the first and the second wiring; and (e) a...

...on the first insulating layer to cover the first wiring, the second wiring, and the **dummy pattern** , the second insulating layer having a cavity embedded in it and shielded thereby between the first or second wiring and the **dummy pattern** .

...Title Terms: **SEMICONDUCTOR** ;
International Patent Class (Main): **H01L-021/768** ...

... **H01L-021/82** ...

... **H01L-023/48**
International Patent Class (Additional): **H01L-021/285** ...
... **H01L-023/12** ...

... **H01L-023/52** ...

... **H01L-029/40**

19/3,K/25 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

010300556 **Image available**
WPI Acc No: 1995-201816/199527
XRAM Acc No: C95-093235
XRPX Acc No: N95-158556
Semiconductor **device of reduced side etching - comprises functional circuit module having wiring** pattern **on substrate with** dummy **wiring** pattern **as first pattern**
Patent Assignee: TOSHIBA KK (TOKE); IWATE TOSHIBA ELECTRONICS KK (IWAT-N)
Inventor: ARAYA B; CHIBA T; CHIDA K; HIRANO Y
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 647966	A1	19950412	EP 94115789	A	19941006	199527	B
JP 7106327	A	19950421	JP 93250493	A	19931006	199527	
KR 155584	B1	19981201	KR 9425286	A	19941004	200031	

Priority Applications (No Type Date): JP 93250493 A 19931006
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 647966	A1	E	7	H01L-021/321	
Designated States (Regional): DE FR GB					
JP 7106327	A		4	H01L-021/3205	
KR 155584	B1			H01L-021/302	

Semiconductor **device of reduced side etching...**

...comprises functional circuit module having wiring pattern **on substrate with** dummy **wiring** pattern **as first pattern**

...Abstract (Basic): **Semiconductor** device comprises a functional circuit module having a wiring pattern on a **semiconductor** substrate with a **dummy** wiring **pattern** of the same material as the first pattern formed in a region close to the...

...USE - Wiring of **semiconductor** device...

...ADVANTAGE - Method reduces side etching and **prevents deterioration** of characteristics and improves reliability
Title Terms: **SEMICONDUCTOR** ;
International Patent Class (Main): **H01L-021/302** ...

... **H01L-021/3205** ...

... **H01L-021/321**

```
Set     Items   Description
S1      16719   AU= (KIM, H? OR KIM H?)
S2    1422888   SEMI()CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE-
            GRATED()CIRCUIT?
S3     764333   CORROSION? OR DECAY? OR RUST? OR DETERIORAT? OR DECOMPOS? -
            OR OXIDI?ATION
S4         70   S1 AND S2 AND S3
S5      26690   (WIRE OR MAIN OR DUMMY OR FINE  OR PAD OR PADS)(2N)PATTERN?
S6          6   S4 AND S5
S7          6   IDPAT (sorted in duplicate/non-duplicate order)
S8          6   IDPAT (primary/non-duplicate records only)
?show files
File 344:Chinese Patents Abs Aug 1985-2002/Sep
         (c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/Jun(Updated 021004)
         (c) 2002 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2002/Sep W05
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20021003,UT=20020926
         (c) 2002 WIPO/Univentio
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200264
         (c) 2002  Thomson Derwent
?
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6/5,K/5 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014762327 **Image available**
WPI Acc No: 2002-583031/200262
XRPX Acc No: N02-462395
Semiconductor **device using damascene technology, comprises** fine **line** patterns **of specific area ratio connected to** pad patterns
Patent Assignee: KIM H (KIMH-I)
Inventor: **KIM H**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020079517	A1	20020627	US 200115757	A	20011217	200262	B

Priority Applications (No Type Date): KR 200080891 A 20001222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020079517	A1		7	H01L-027/10	

Abstract (Basic): US 20020079517 A1
NOVELTY - The **semiconductor** device comprises several aluminum/copper metal **wire patterns** , each of which includes **fine** line **pattern** connected to **pad patterns** through connection **pad patterns** . The area ratio of the **fine** line **pattern** to an overall **wire pattern** is greater than 1%.
USE - **Semiconductor** device using damascene technology.
ADVANTAGE - The specific area ratio set for the **fine** line **patterns** , prevents the pattern from **corrosion** .
DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the patterns formed on the **semiconductor** device.
pp; 7 DwgNo 4/4
Title Terms: **SEMICONDUCTOR** ; DEVICE; TECHNOLOGY; COMPRISE; FINE; LINE; PATTERN; SPECIFIC; AREA; RATIO; CONNECT; PAD; PATTERN
Derwent Class: U11
International Patent Class (Main): H01L-027/10
File Segment: EPI

Semiconductor **device using damascene technology, comprises** fine **line** patterns **of specific area ratio connected to** pad patterns
Inventor: **KIM H**

Abstract (Basic):
... The **semiconductor** device comprises several aluminum/copper metal **wire patterns** , each of which includes **fine** line **pattern** connected to **pad patterns** through connection **pad patterns** . The area ratio of the **fine** line **pattern** to an overall **wire pattern** is greater than 1%.
... **Semiconductor** device using damascene technology...

...The specific area ratio set for the **fine** line **patterns** , prevents the pattern from **corrosion** .
...

...The figure shows a schematic view of the patterns formed on the **semiconductor** device
Title Terms: **SEMICONDUCTOR** ;